

1 **ABSTRACT**

2 Disclosed herein are circuits in which a plurality of clock signals are
3 generated by corresponding clock generators from one or more common clock
4 references. The clock generators accept control values that specify the phases of
5 the individual clocks. The actual phase of each clock signal potentially varies
6 during operation, and the phases of the various clock signal are generally
7 independent of each other. To detect or measure phase relationships, the disclosed
8 circuits evaluate or compare the control values using arithmetic logic.
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